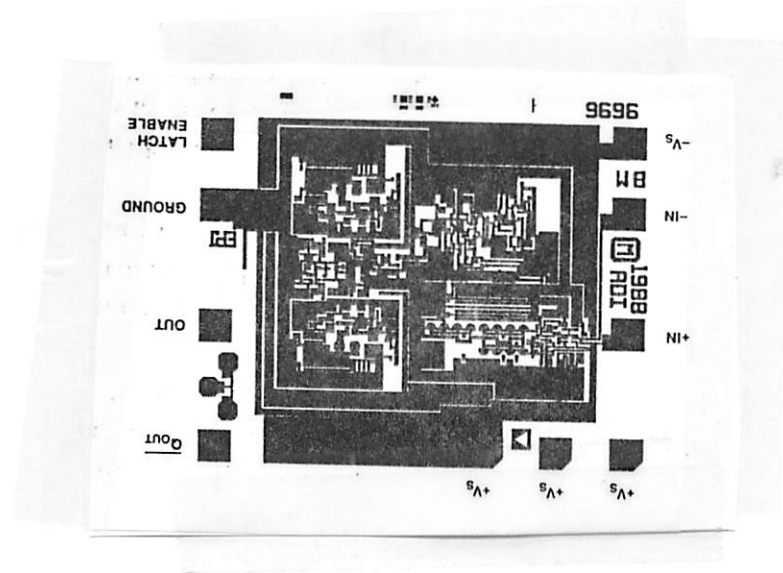




# Sierra Components, Inc.

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Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**Topside Metal: Al (Aluminum)**

**Backside: Si**

**Backside Potential: -Vs**

**Mask Ref:**

**Bond Pads (Mils): 4 X 4**

**APPROVED BY:**

**MFG: AD**

**DIE SIZE (Mils): 59 X 71**

**THICKNESS: 15**

**DATE: 3/2/00**

**P/N: AD9696**

DG 10.1.2  
Rev A 3-4-99